

Patent Claims

1. Method for producing an integrated semiconductor component comprising the steps:

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- a) a semiconductor substrate having at least one first region and at least one second region is prepared;
- b) gate paths are produced in the first and in the second region of the semiconductor substrate;
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- c) source/drain regions neighboring the gate paths and at least two spacers at the gate paths are produced in the first region of the semiconductor substrate;
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- d) source/drain regions are produced neighboring the gate paths in the second region of the semiconductor substrate, and, for preparing the contacts to predetermined source/drain regions in the second region of the semiconductor substrate, sacrificial contacts are formed before all spacers have been produced in the first region of the semiconductor substrate.

2. Method according to claim 1, characterized in that the spacers are formed of silicon oxide, silicon nitride or oxynitride.

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3. Method according to claim 1 or 2, characterized in that the gate paths are formed in that a polysilicon layer and a protective layer, particularly a silicon nitride, silicon oxide or oxynitride layer, are generated and these layers are structured in common to form gate paths.

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4. Method according to claim 3, characterized in that the protective layer is generated with a thickness such that the protective layer exhibits a thickness of less than 100 nm after the gate structuring.

5. Method according to one of the preceding claims, the gate paths in the first region of the semiconductor substrate are doped with dopants having different conductivity types.

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6. Method according to one of the preceding claims, characterized in that silicide layers are generated on the gate paths in the first region of the semiconductor substrate.

~~7. Method according to claim 6, characterized in that CoSi_2 , TaSi_2 , TiSi_2 or WSi_x are employed as silicide layers.~~

8. Method according to claim 6 or 7, characterized in that the silicide layers are produced with a salicide method.

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